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Abstract of the Disclosure

An apparatus and method for selectively converting a clock frequency in a digital signal receiver. The apparatus includes: a first phase locked loop (PLL); a second phase locked loop; a switching portion for selecting a clock frequency from one of the first and second phase locked loops according to a predetermined control signal; and a controller for controlling the switching portion to select and output the clock frequency corresponding to the frame rate of an input digital signal. The frame rate of an input digital signal is detected and the clock frequency which corresponds to the detected frame rate is provided to only the blocks for the corresponding signal process. Also, in the case where an analog NTSC signal is input, the corresponding clock frequency can be provided to only the blocks associated with the corresponding signal process. Thus, omission or redundancy in video signal processing can be prevented.